环形正负电子对撞机
Circular Electron Positron Collider

中国科学院高能物理研究所
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CENTRAL CHINA NORMAL UNIVERSITY

Development of high granularity digital pixel sensors for the CEPC Vertex Detector

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on behalf of the CEPC VTX study group

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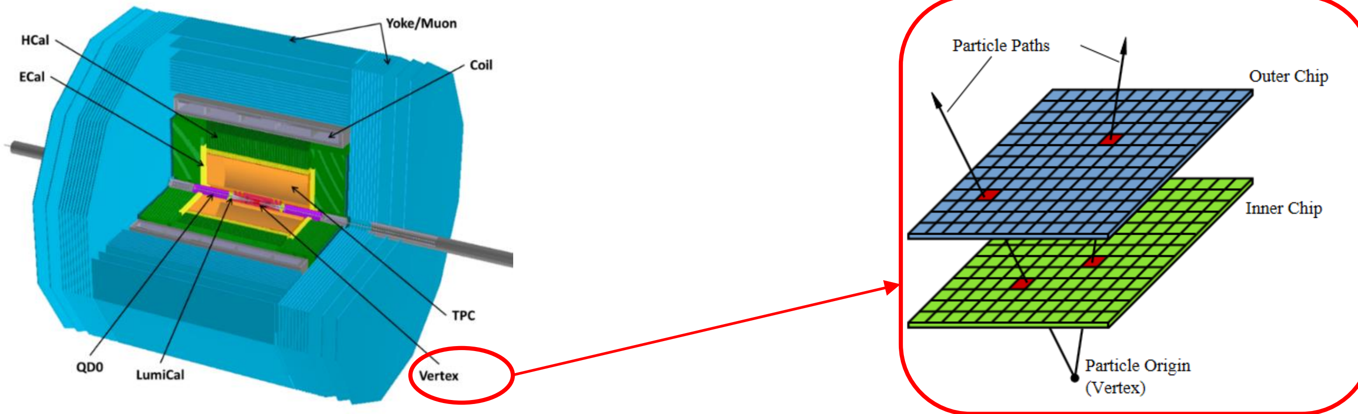
Outline

- ❖ **From physics driven requirements to sensor design specifications**
- ❖ **High granularity digital pixel prototypes for CEPC R&D**
  - ❑ **JadePix2** & **MIC4** in CMOS technology
  - ❑ **CPV1/2:** in SOI technology
- ❖ **Summary and outlooks**
- ❖ **Acknowledgement**

Physics driven requirements



- **Efficient tagging of heavy quarks (b/c) and τ leptons:**

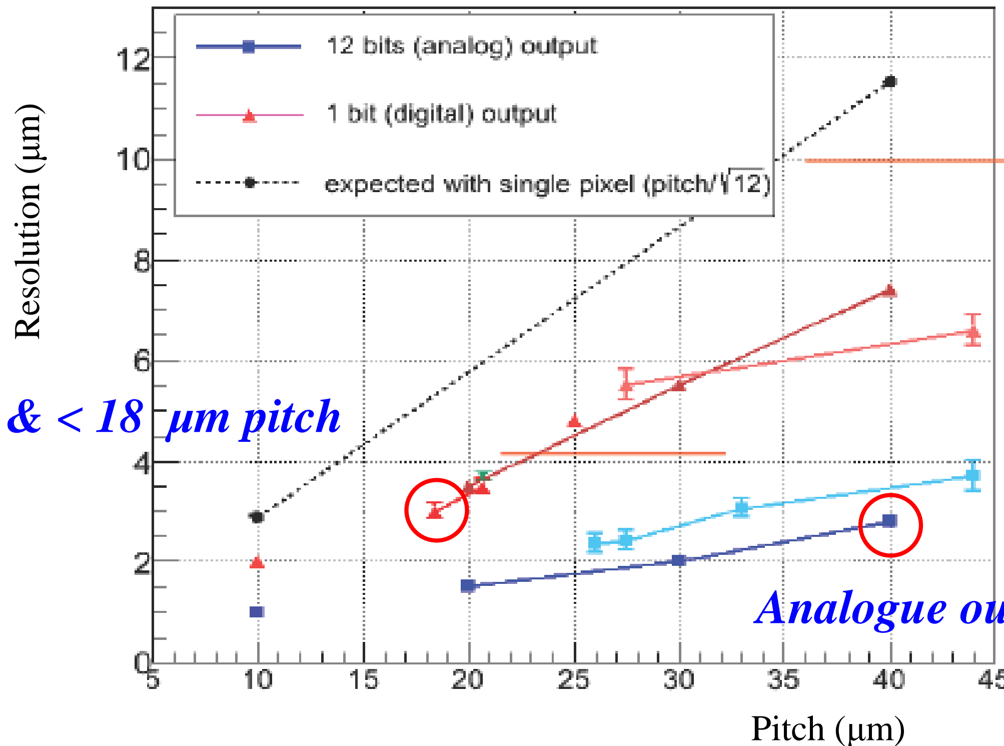
  Impact parameter resolution: $\sigma_{r\phi} = a \oplus \frac{b}{(p \cdot sin^{3/2}\theta)}\ \mu m$

  a *depends on single point resolution $\sigma_{s.p.}$ & on the lever arm*
  b *depends on the distance between the innermost layer to IP and on the material budget*

- **Design constrains on vertex (to achieve a =5 , b = 10, and B= 3T):**
  - Spatial resolution near the interaction point $\leq 3\ \mu m$
  - Material budget $\leq 0.15\%\ X_0/layer$
  - First layer located at a radius *~1.6 cm*
  - Detector occupancy $<1\%$

Design goal: $\sigma_{sp} < 3\ \mu m$

How to reach:* $\sigma_{sp} < 3\ \mu m$? [+]: *either a small pixel size or more data information

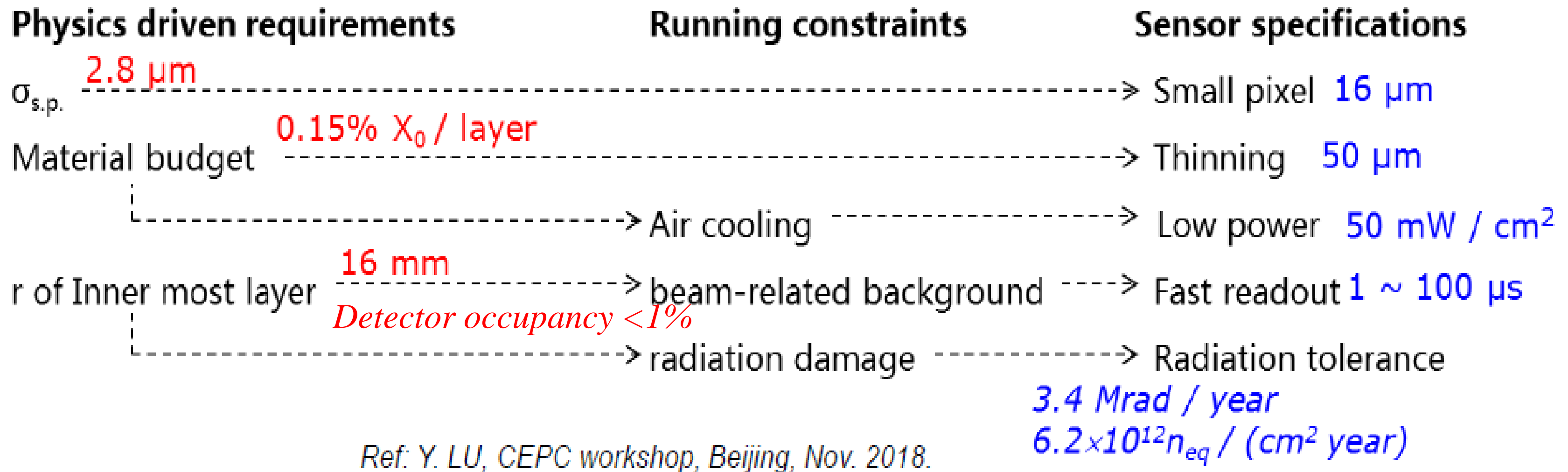


Spatial resolution vs pitch obtained from Mimosa* sensors @ *IPHC*

For CEPC: Binary output, with digitization electronics integrated into each pixel < 18 μm pitch size

[+] *J.Baudot, "**An ILD vertex detector with CMOS sensor –status report**", in Linear Collider Power Distribution and Pulsing workshop, LAL Orsay, May 2011.*

Sensor design Specifications



Difficulty: meet all the specifications at the same time.

Promising technologies:

HR-CMOS pixel sensor

DEPFET

SOI pixel sensor

3D-IC

High granularity digital pixel prototypes for CEPC

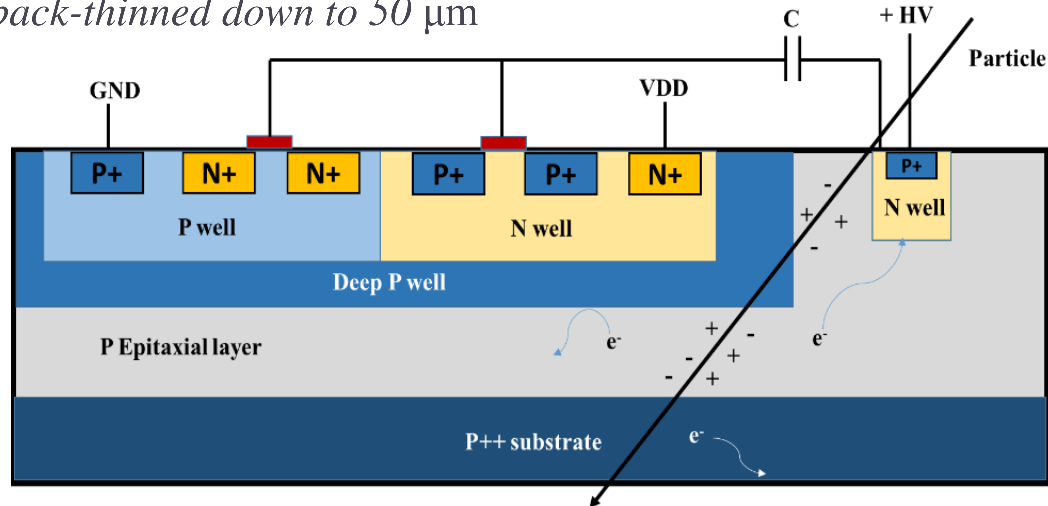
Prototype	Technology	Pixel size (μm^2)	Collection diode bias (V)	Matrix size	R/O architecture
MIC4	0.18μm HR-CMOS	25×25	-1 — -6V	128×64	Asynchronous
JadePix2		22×22	1 — 10V	96×112	Rolling shutter
CPV1/2	0.2μm SOI	16×16	< - 40 V	64×64	

To achieve a digital pixel size as compact as possible, while maintaining other specifications (power, speed)

MIC4: technology

CMOS technology: *TowerJazz 0.18 μm CIS process*

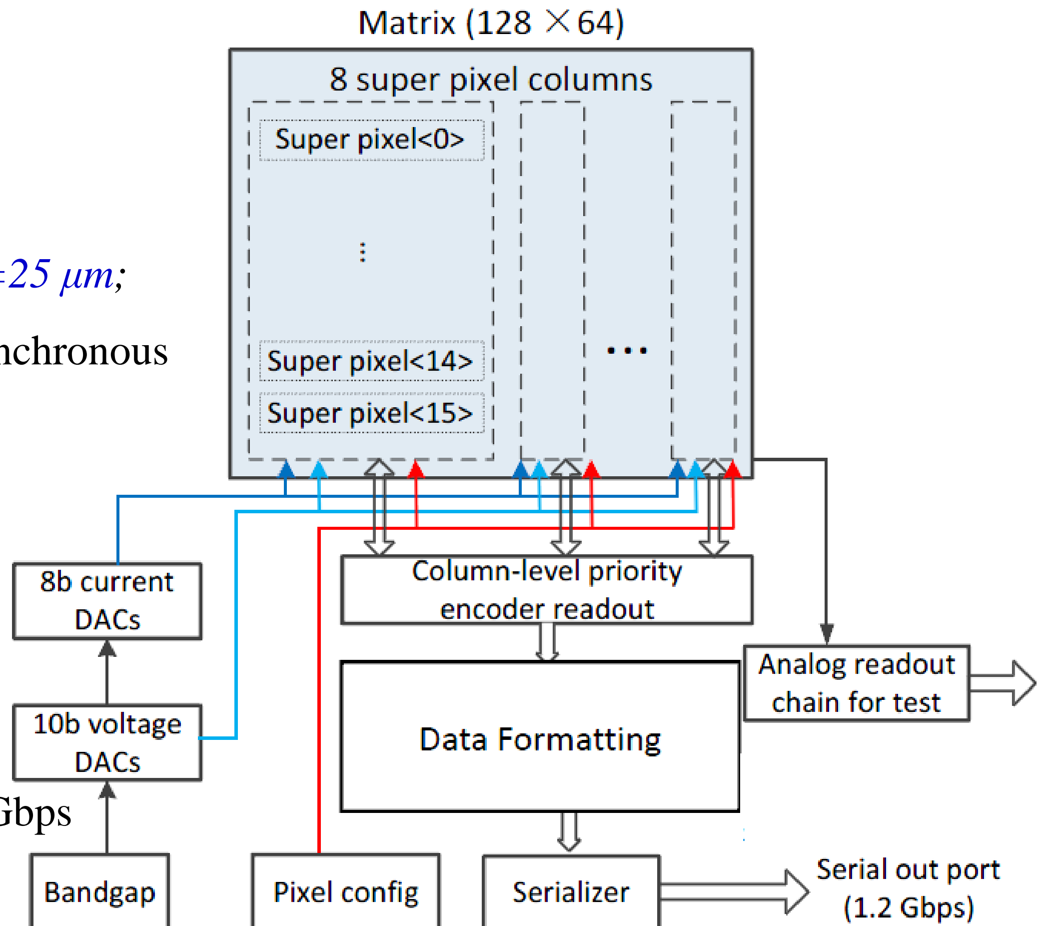
- Quadruple well process, deep PWELL shields NWELL of PMOS: full in-pixel CMOS
- Thick (~20 μm) and high resistivity (≥1 kΩ•cm) epitaxial layer: more depletion
- *Thin gate oxide (<4 nm): robust to total ionizing dose*
- *6 metal layers: layout benefited*
- *Could be back-thinned down to 50* μm



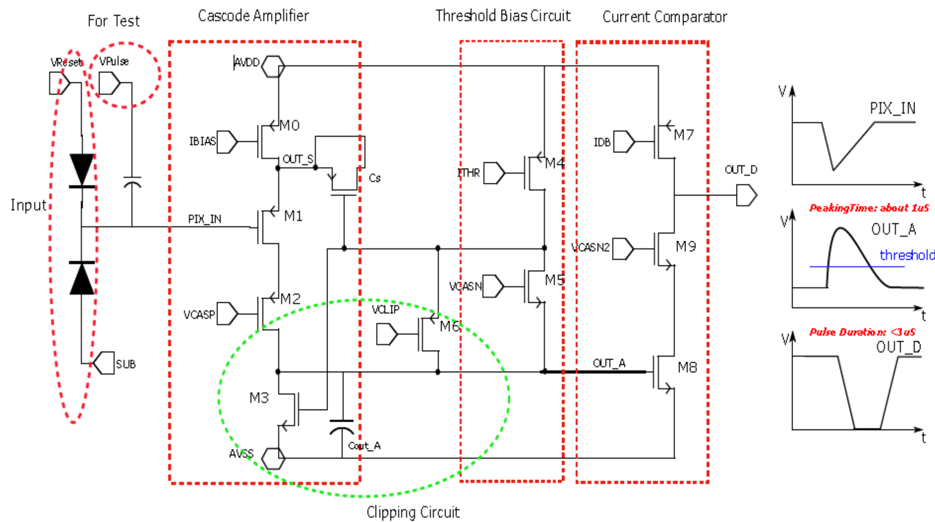
- *Latest Mimosa series @ IPHC for STAR*
- *ALPIDE @CERN for ALICE upgrade*

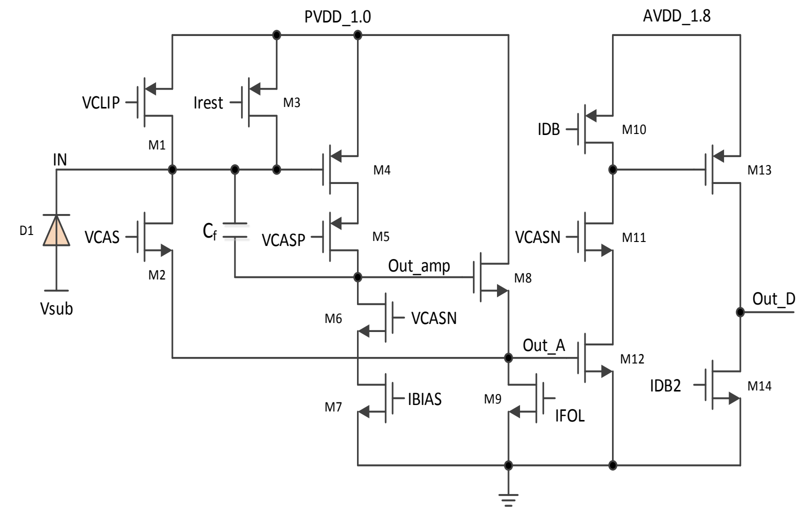
MIC4: overview

- Chip overview:
  - *3.1 × 4.6 mm²; 128 × 64 pixels*
  - *2 Pixel front-end versions,*
  - *both two pixel versions pitch size=25 μm;*
  - Processing speed: data-driven asynchronous
    - 25 ns/pixel;
  - Matrix Power:
    - < 20 mW/cm² ;
  - Data driven readout:
    - Real time readout
    - High speed data link of 1.2 Gbps



MIC4: in-pixel front-end

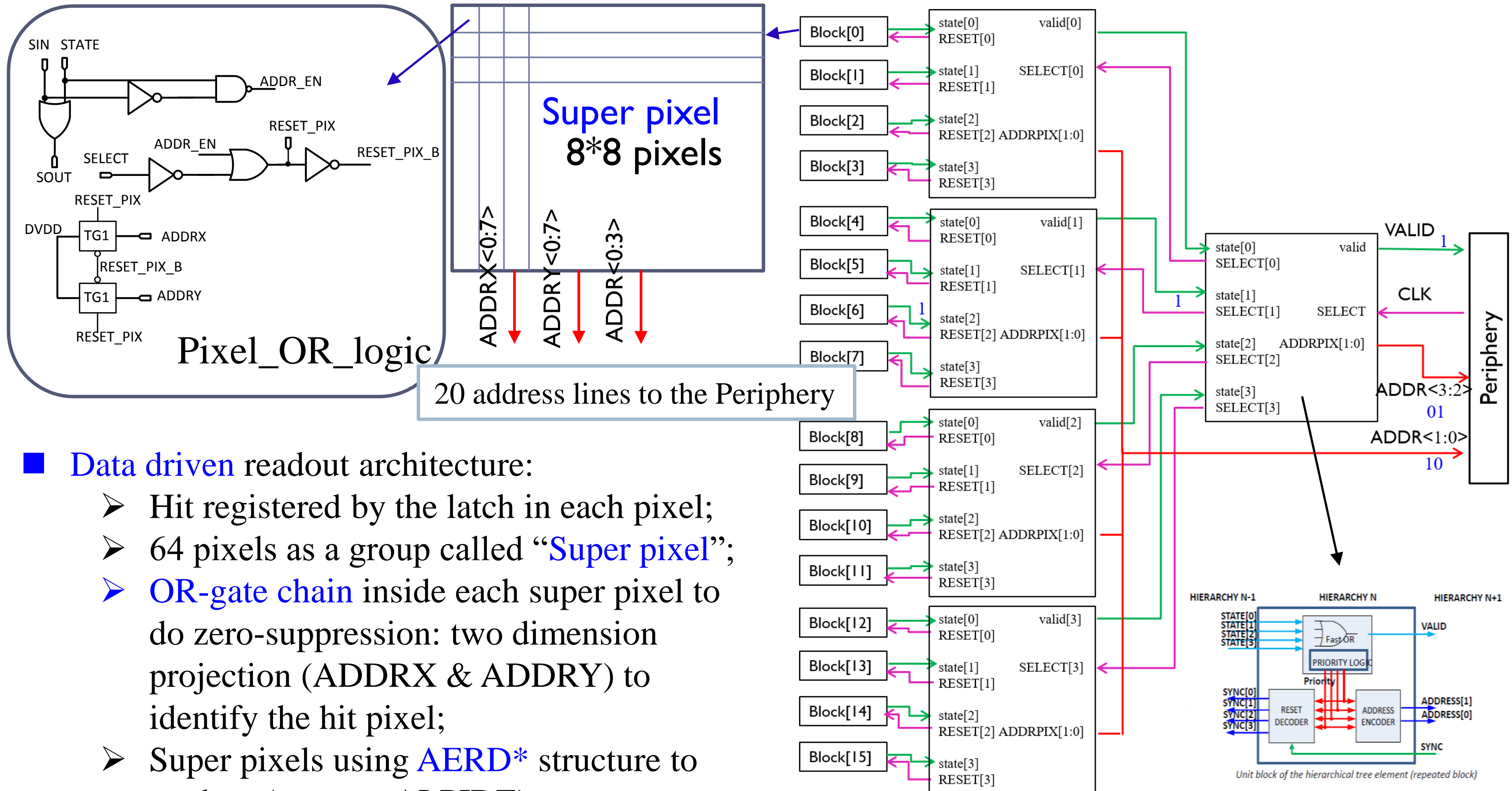




- Version 1:
  - Same structure as ALPIDE* (@CERN, for ALICE upgrade), with different parameters
  - Peaking time < 1μs, pulse duration < 3 μs, 110 nW/pixel (increased by a factor of 3)
- Version 2:
  - CSA based front-end, feedback capacitance 0.2fF
  - Peaking time < 1μs, pulse duration < 10 μs, 50 nW/pixel

* Ref.: D. Kim et al., 2016 JINST 11 C02042

MIC4: readout architecture

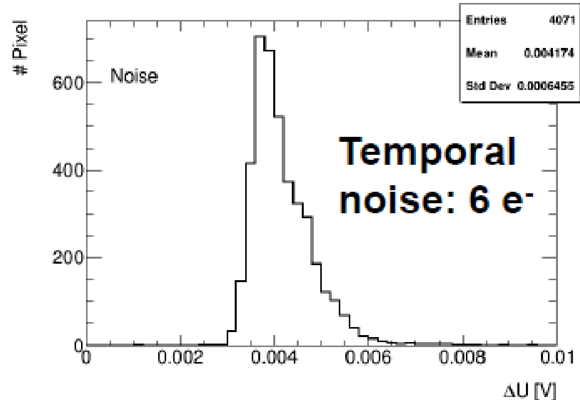


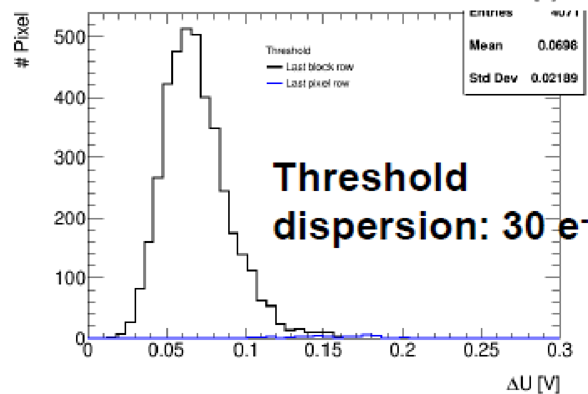
- Data driven readout architecture:
  - Hit registered by the latch in each pixel;
  - 64 pixels as a group called "Super pixel";
  - OR-gate chain inside each super pixel to do zero-suppression: two dimension projection (ADDRX & ADDRY) to identify the hit pixel;
  - Super pixels using AERD* structure to readout (same as ALPIDE)

*AERD readout scheme(Address Encoder Reset Decoder)

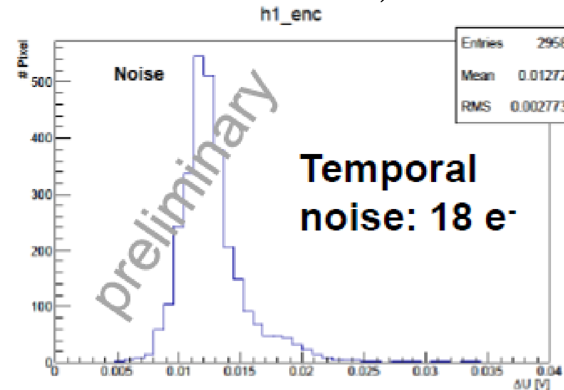
MIC4: test results

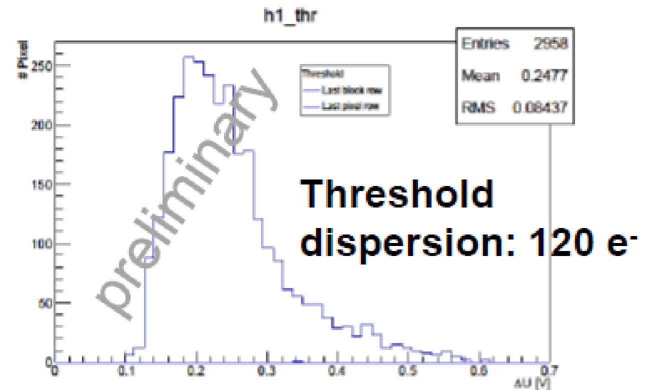
- Pixels with FE version1:
  - TN: ~ 6 e⁻;
  - FPN: ~ 30 e⁻;





- Pixels with FE version2:
  - TN: ~ 18 e⁻;
  - FPN: ~ 120 e⁻;

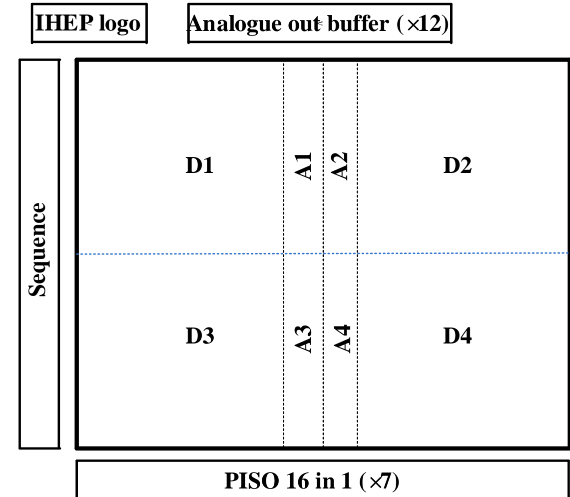




JadePix2: overview

Chip overview:

- *3 × 3.3 mm^2; 96 × 112 pixels with 8 sub-matrix*
- *Two pixel versions: both pitch size=22 µm*
- Processing speed: rolling shutter mode
  - 100 ns/row (version 1);
  - 80 ns/row (version 2);
- Power:
  - 3.7 µA/pixel (version 1);
  - 6.5 µA/pixel (version 2);
- Data:
  - Binary output: 16-to-1 serializer,
LVDS transmitter @160MHz clock
  - Analogue output: 4 column pixels for each version

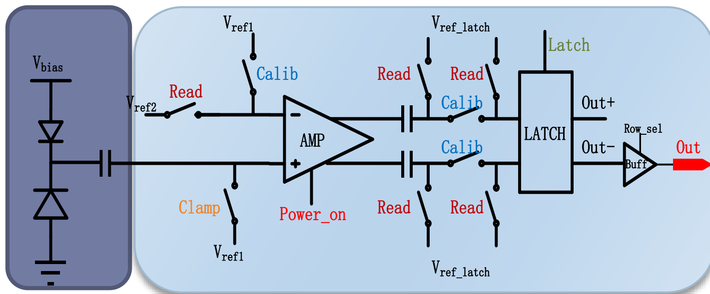


Floorplan of JadePix2

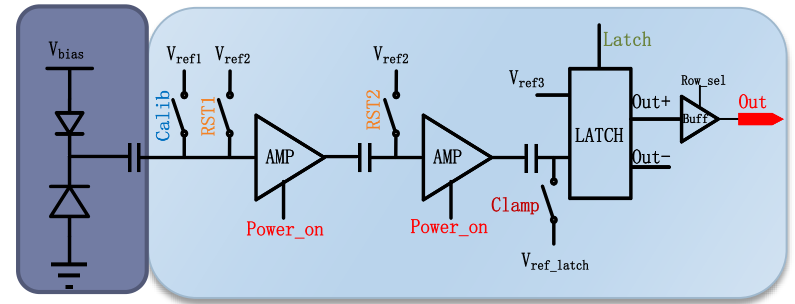
<table>
<tr><th></th><th>D1</th><th>A1</th><th>A2</th><th>D2</th><th>D3</th><th>A3</th><th>A4</th><th>D4</th></tr>
<tr><td>Diode size</td><td colspan="4">4 µm²</td><td colspan="4">8 µm²</td></tr>
<tr><td>Design Version</td><td colspan="2">2: Single-end</td><td colspan="2">1: Differential</td><td colspan="2">2: Single-end</td><td colspan="2">1: Differential</td></tr>
<tr><td>Matrix size:
①48 row×44 col.
②48 row×4 col.
③48 row×60 col.</td><td>①</td><td colspan="2">②</td><td>③</td><td>①</td><td colspan="2">②</td><td>③</td></tr>
</table>

JadePix2: in-pixel structures and operation timing

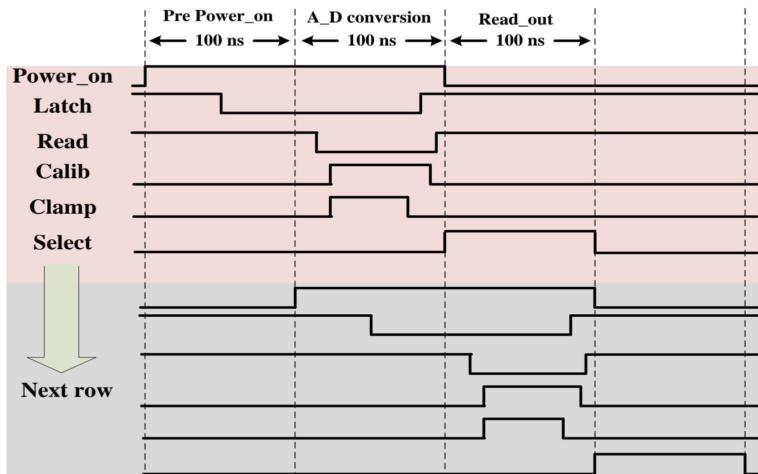
2 pixel versions: in-pixel offset cancellation and high precision comparator



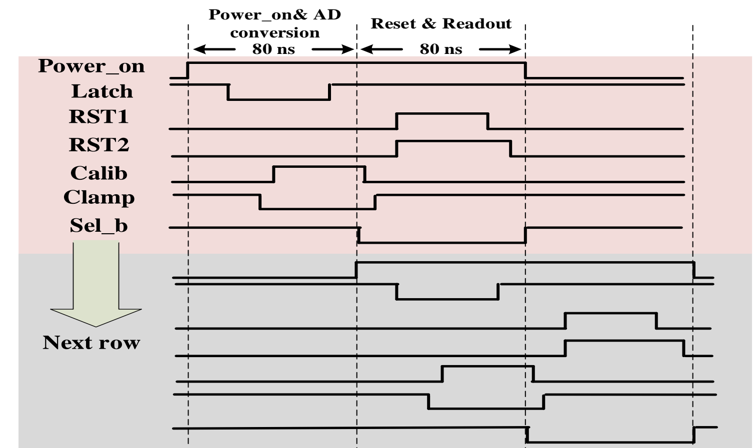
Version 1: differential amplifier + latch



Version 2: two stage CS amplifiers + latch



Operation timing of pixel version 1

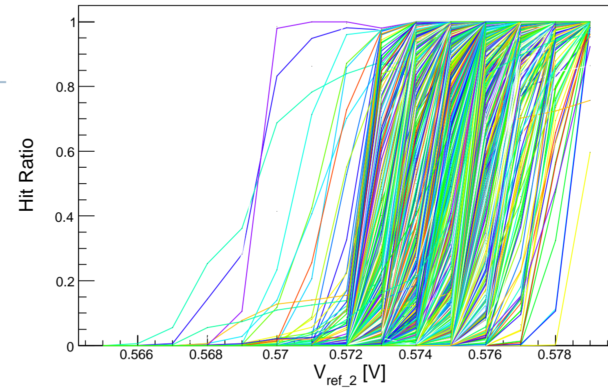


Operation timing of pixel version 2

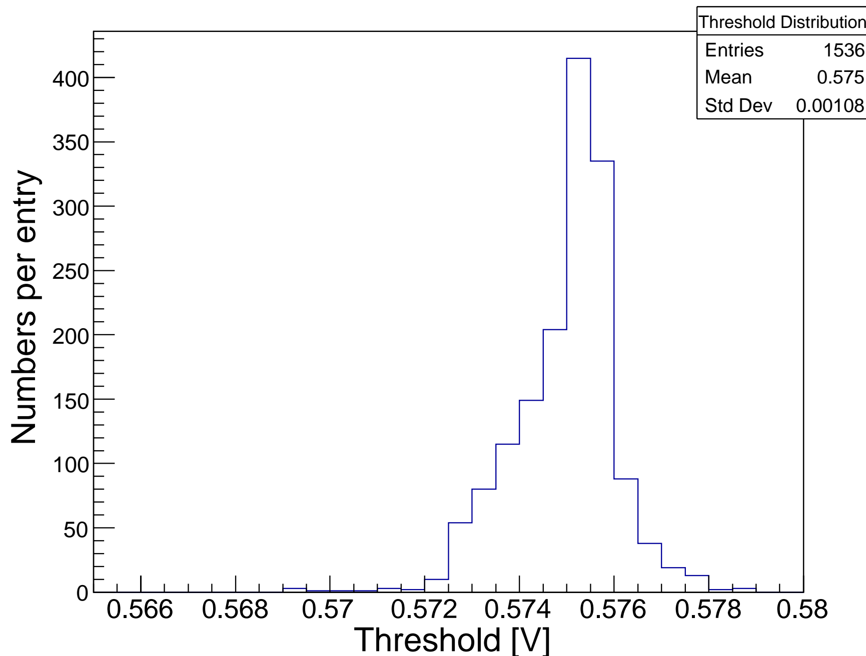
JadePix2: test results 1/2

S-curve measured on pixel version 1:

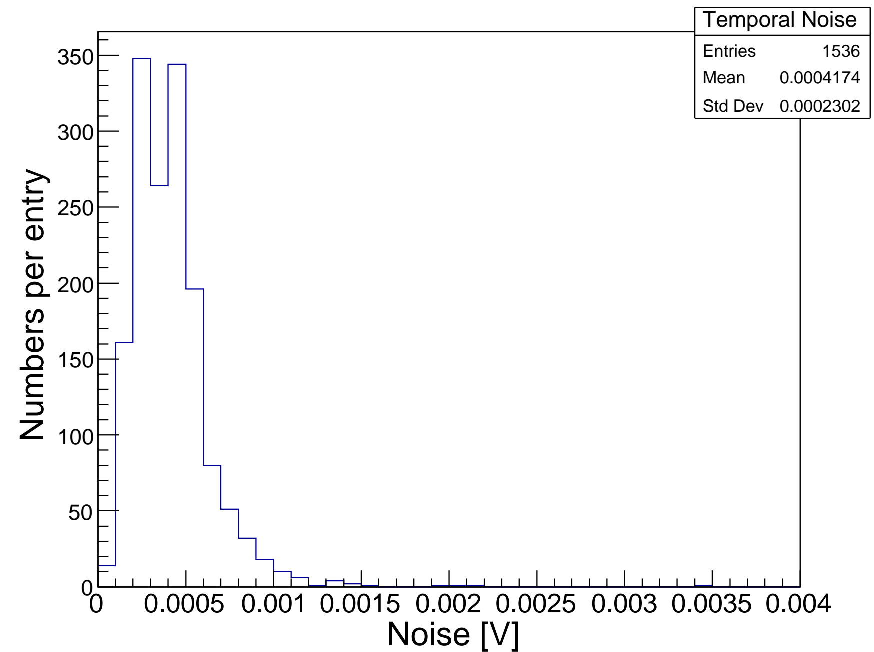
$$\text{Total ENC} = \sqrt{29^2 + 11^2} = \sim 31\ e^-$$



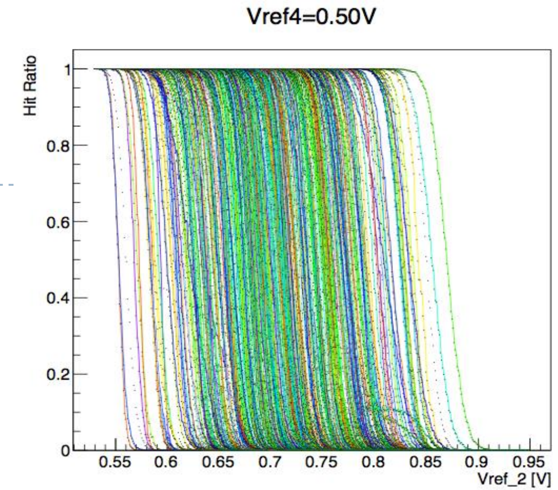
FPN: 1.08mV @input node ENC: ~29 e^-



TN: 0.4mV @input node ENC: ~11 e^-



JadePix2: test results 2/2

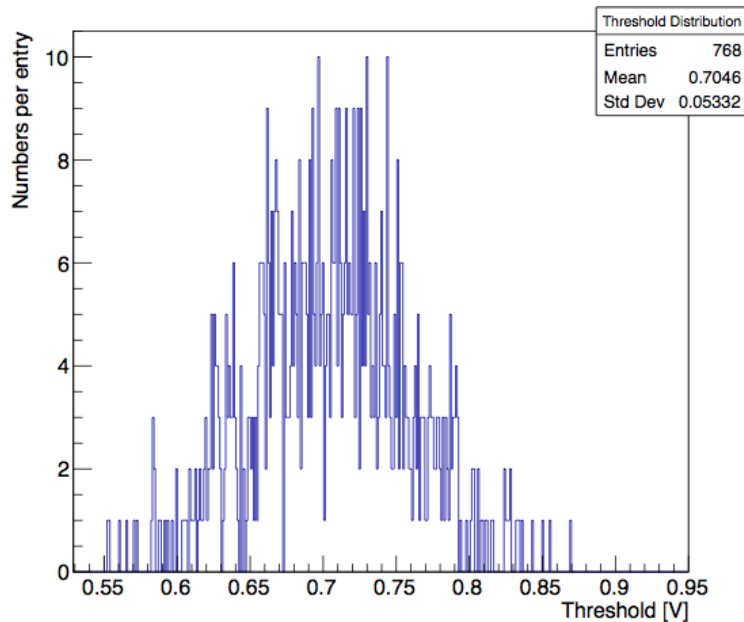


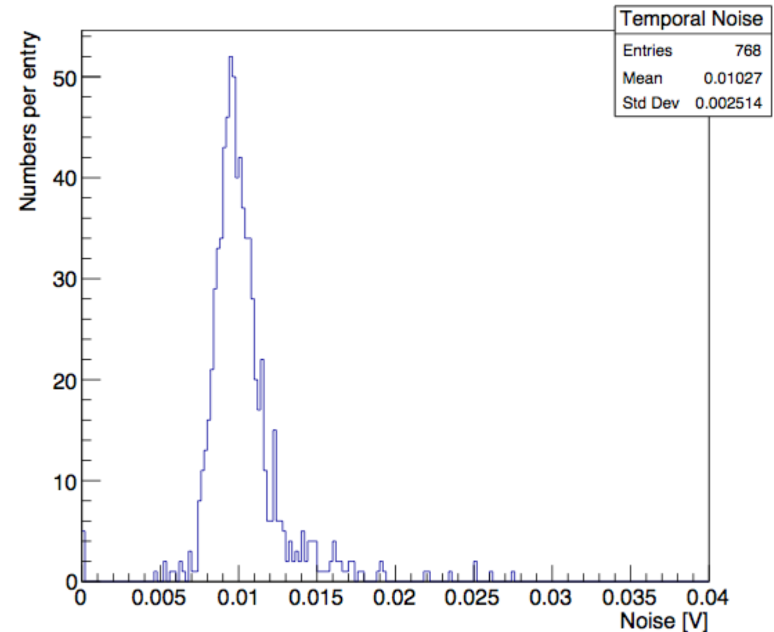
S-curve measured on pixel version 2:

$$\text{Total ENC} = \sqrt{29^2 + 5.5^2} = \sim 30\ e^-$$

FPN: 53/52(G_a)=1.02mV @input node ENC: ~29 e^-

TN: 0.2mV @input node ENC: ~5.5 e^-

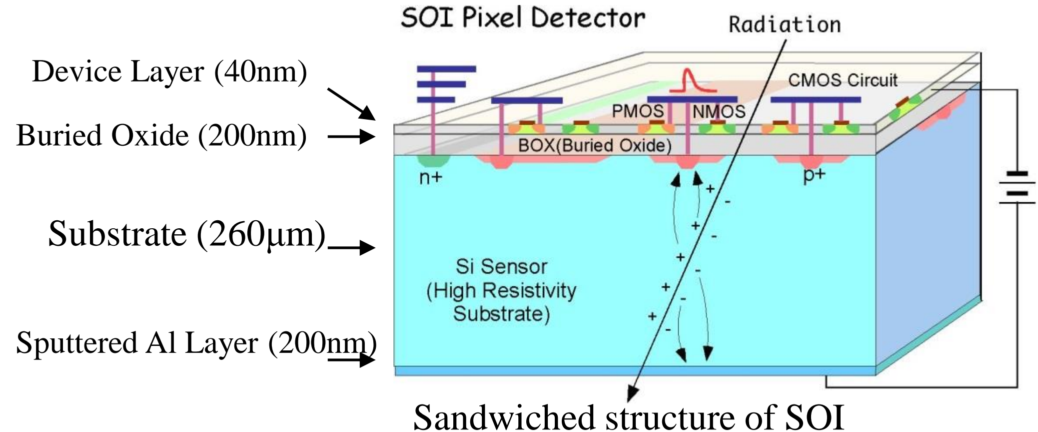




CPV: technology

SOI: *LAPIS 0.2um process*

- Fully depleted sensor
- Full in-pixel CMOS
- 5 Metal layers
- High resistive substrate (≥1 kΩ•cm).
- Could be back thinned down to 75 µm

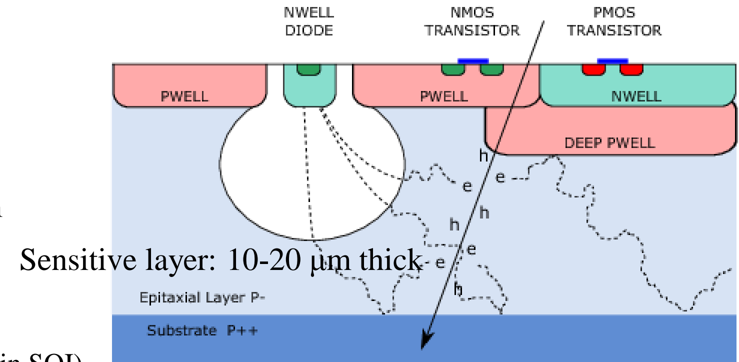


Sandwiched structure of SOI

Concerning about granularity

SOI pixel technology potential advantages:

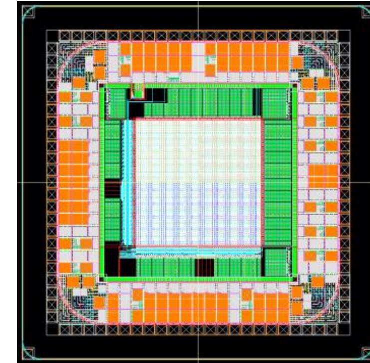
- Thicker sensitive layer: *simplify the electronic design*
  - 2-3 times signal charges for MIP even after back thinning down to ≈ 50µm
- More compact layout: *shrink the pixel size*
  - PMOS & NMOS transistor could be closer (no NWELL PWELL used for transistors in SOI)



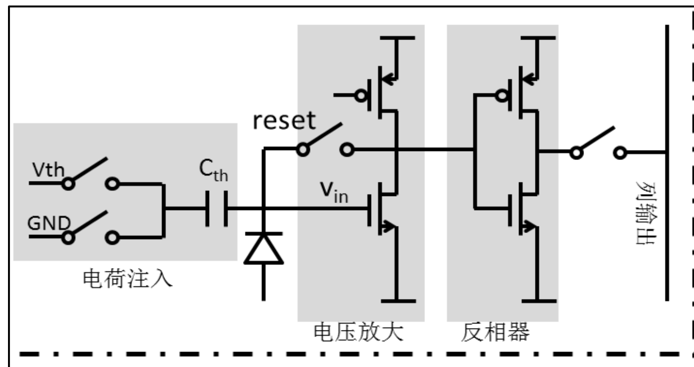
CMOS technology

CPV1: overview

- First digital pixel of 16um pitch size
- CS voltage amplifier, gain ~ 10
- Inverter as discriminator
- Threshold charge injected to sensing node
- Pixel array: 64*32 (digital) + 64*32 (analog)
- Double-SOI process for shielding and radiation enhancement
- Submitted June, 2015

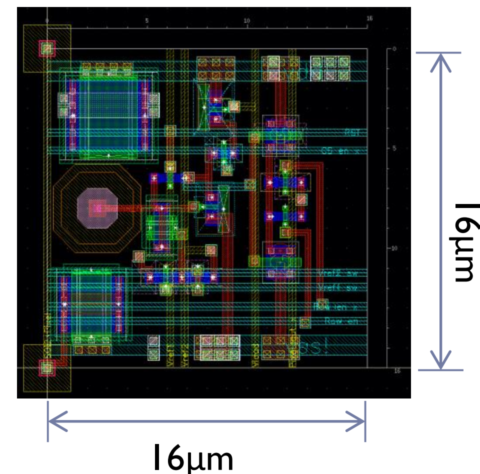


CPV1 prototype layout: *3 × 3 mm²*



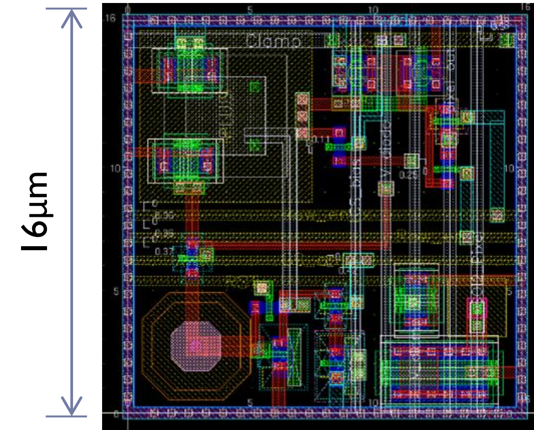
Pixel schematic of CPV1

CPV1 digital pixel layout

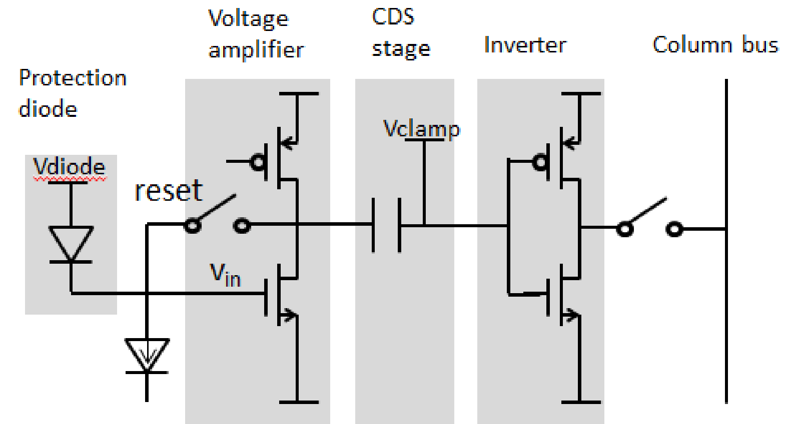


CPV2: overview

- 3×3 mm², with 64×64 pixel array, 16 µm pixel pitch
- Readout: rolling-shutter
  - 100ns/row
- Protection diode added
  - Enable full depletion on sensor
- In-pixel CDS stage inserted
  - improved RTC and FPN noise
  - replaced the charge injection threshold
- Sensor thickness was thinned to 75 µm
- Submitted June, 2016



CPV2 digital pixel layout

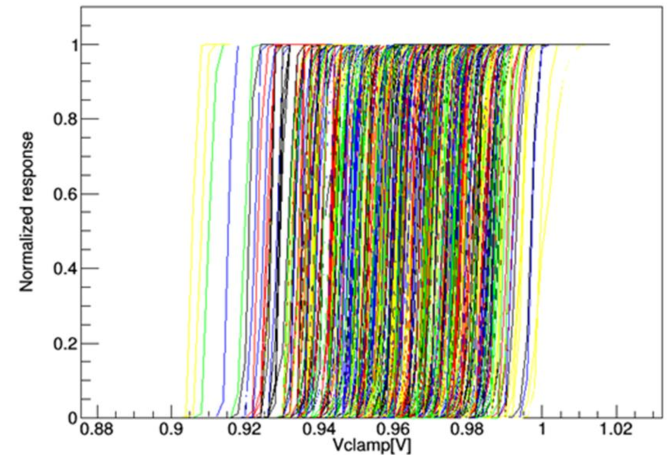


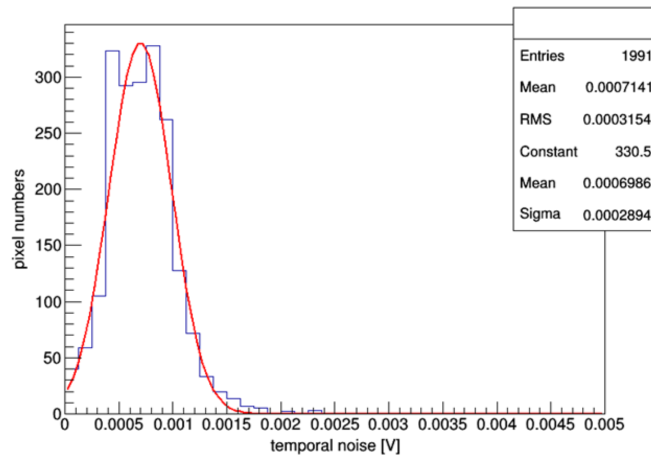
Pixel schematic of CPV2

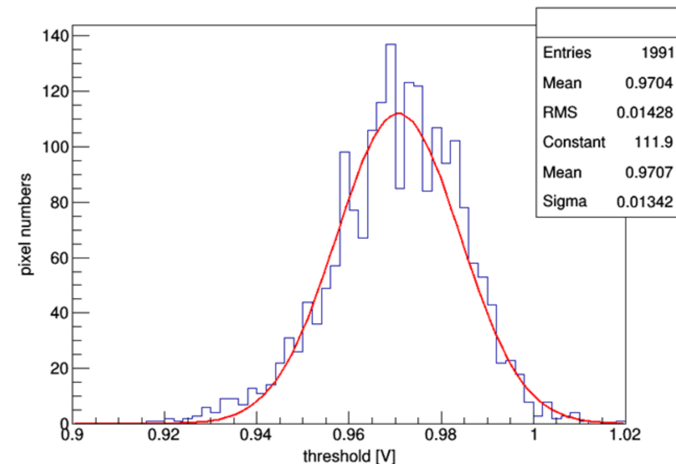
CPV2: noise performances

- Full depletion confirmed with ^{55}Fe and Infrared laser respectively at $V_{bias} < -30V$
- Calibration with ^{55}Fe 5.9keV X-ray, CVF = 123.3μV/e-
- Noise performances
  - TN: ~6e$^-$
  - FPN:~114e$^-$; need to be improved.

Digital pixel array S-Curve

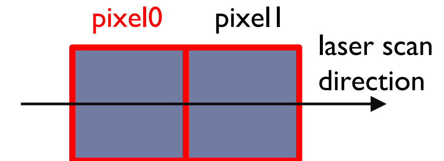


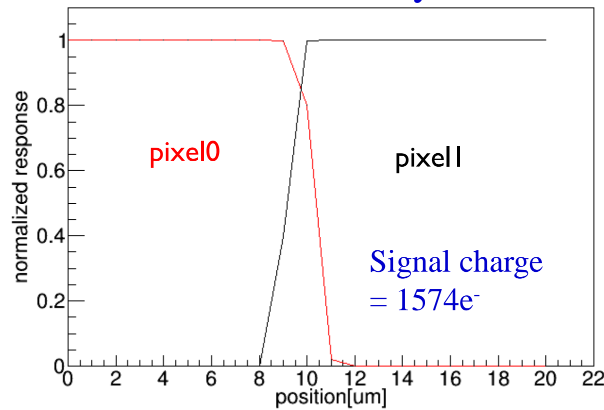


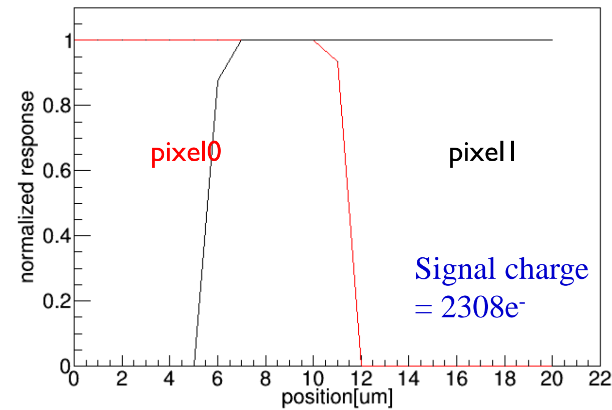


CPV2: laser position scan with different intensity

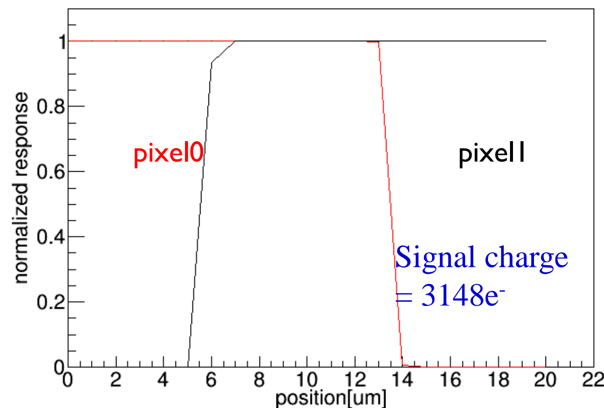
- Scan across two adjacent digital pixels
  - Step size: 1μm
  - Threshold is fixed at minimum value without noise hits
  - Different beam intensity is used

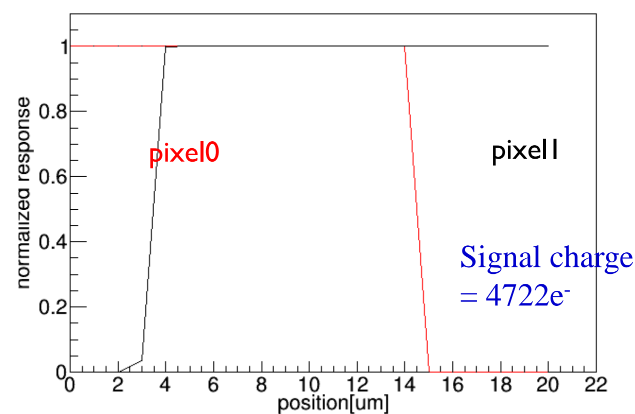






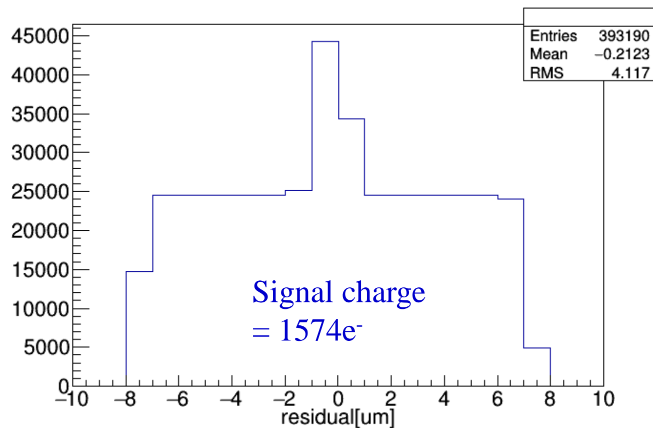
Normalized response =number of hit/number of pulse

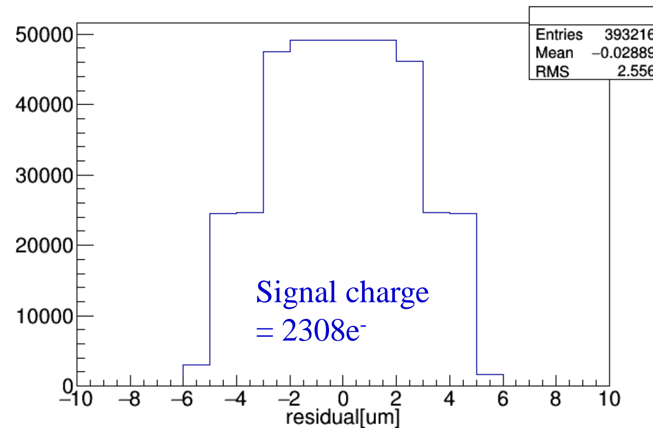




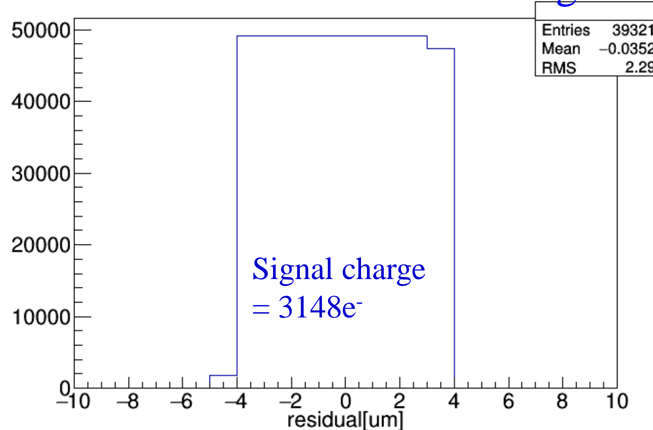
CPV2: spatial resolution by laser

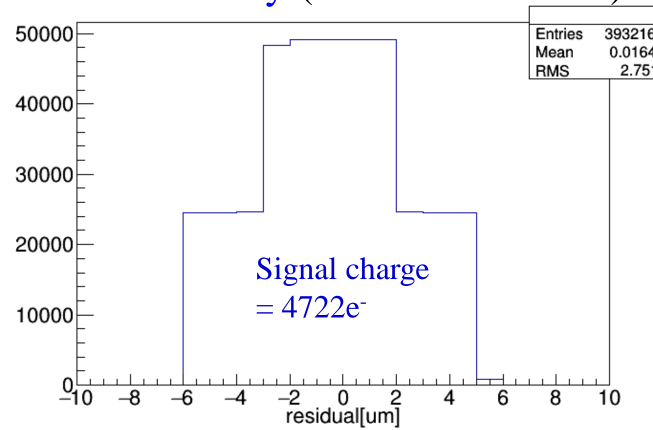
- Responding position reconstructed by Center of Gravity; RMS value of residual distribution indicates its single point resolution





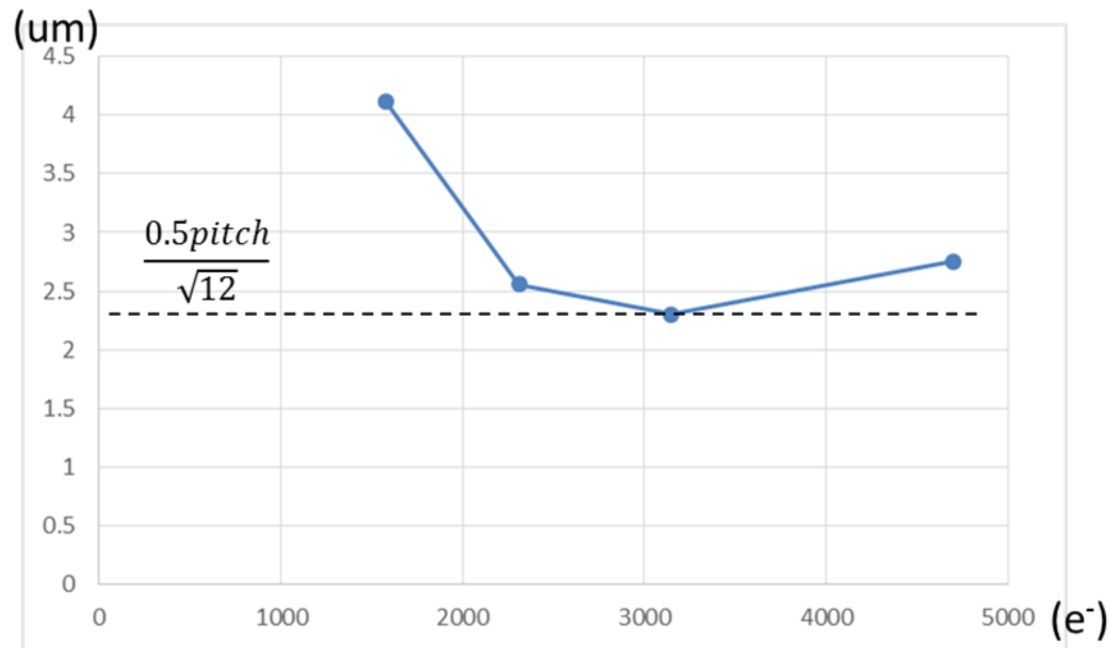
Residual distribution changes with beam intensity (threshold is fixed)





CPV2: spatial resolution by laser

- Single point resolution versus signal charge
  - Get the best resolution of 2.3µm at ~ 3000e⁻ signal level



Summary

- A variety of pixel prototypes has been designed for CEPC R&D, on the specifications of high spatial resolution, low power and fast readout.
- Spatial resolution < 3μm has been demonstrated on CPV2, with 16 μm digital pixel pitch size;

Prototype	Technology	Pixel size (μm²)	Collection diode bias (V)	Noise (e⁻)	R/O architecture	Readout time (μs) for ~1.5×3.0 cm²
MIC4	0.18μm HR-CMOS	25×25	-1 — -6V	~30	Asynchronous	< 10 μs
JadePix2		22×22	1 — 10V	~30	Rolling shutter	~ 60 μs
CPV2	0.2μm SOI	16×16	< - 30 V	~114		~ 80 μs

Outlooks

- Explore novel readout scheme
- Design prototypes with large pixel matrix
- Radiation hardness study
- Explore 3D integration technology or new process with smaller feature size

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C. Gao, X. Huang, Y. Li, J. Liu, W. Ren, X. Sun, B. You, L. Xiao, P. Yang, D. Zhang, L. Zhang, W. Zhou

Thanks for your attention!

Speed

	H(240)	W(160)	Z(91)
Hit density (hits $\cdot$ cm^{-2} $\cdot$ BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

size. Here we assume 10 μs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit, where a pixel is taken to be 16×16 μm^2. The resulting

Power

Vertex detector	Power dissipation	Cooling method	Material budget requirement/layer
Alice ITS	300 mW/cm^2	water	0.3%
STAR PXL	170 mW/cm^2	air	0.39%
ILD vertex	<120mW/cm^2 (CPS and DEPFET)	air or N_2	0.15%
	35W inside cryostat (FPCCD)	two-phase CO_2	

Radiation tolerance

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2$\cdot$BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2$\cdot$year]	2.1	5.5	6.2

Table 9.4: Summary of hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer (r = 1.6 cm) at different machine operation energies of $\sqrt{s}$ = 240, 160 and 91 GeV, respectively.